DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michele Connell (Reg. No. 52,763) on 6/30/2008.

The application has been amended as follows:

Claims 3-6, 8, 12, 14 and 15 are canceled.

Claim 7 (Currently Amended) An image processing circuit, comprising:

a color sensitivity correction circuit which adds or subtracts a predetermined offset to or from a pixel signal obtained, for each column, by amplifying photoelectric conversion signals of pixels, and multiplies a result of the addition or subtraction by a predetermined gain, said pixels having a photoelectric conversion element respectively and being arranged in column and row directions,

wherein said predetermined offset includes a first offset, which is set according to each color, and a second offset, which is set according to a plurality of columns, and

wherein said color sensitivity correction circuit comprises an offset generation section, which compares pixel signals for each column with a reference value corresponding to brightness of at least one frame of an image, dynamically generates the second offset according to the result of the comparison, and updates the dynamically generated second offset as the second offset[[.]], wherein said reference value is determined based on a gain of an amplifier for amplifying said pixel signals corresponding to at least one frame of an image.

Claim 9 (Currently Amended) An image processing circuit, comprising:

a correction circuit for or adding or subtracting an offset for each column, which is set according to a plurality of columns, to or from pixel signals obtained for each column by amplifying photoelectric conversion signals of pixels, said pixels having photoelectric conversion elements and being arranged in column and row directions,

wherein said correction circuit further comprises an offset generation section which compares the pixel signals for each column with a reference value corresponding to brightness of at least one frame of an image, generates said offset for each column dynamically according to the result of the comparison, and updates the dynamically generated offset for each column as the offset for each column[[.]], wherein said reference value is determined based on a gain of an amplifier for amplifying said pixel signals corresponding to at least one frame of an image.

Claim 16 (Currently Amended) A color image sensor, comprising: the image processing circuit according to any one of claims 2[[,]] and 9-11 ~~and 15~~;

a pixel array where said pixels are arranged in column and row directions; and

a column output circuit which is disposed for each column, amplifies the photoelectric conversion signals of said pixels arranged in the column direction; and outputs said ~~image~~ pixel signals.

Allowable Subject Matter

2. Claims 2, 7, 9-11 and 16 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Regarding claim 7, the prior art of record fails to teach or fairly suggest the combination of all limitations of claim 7 that includes **"said color sensitivity correction circuit comprises an offset generation section, which compares pixel signals for each column with a reference value corresponding to brightness of at least one frame of an image, dynamically generates the second offset according to the result of the comparison, and updates the dynamically generated second offset as the second offset, wherein said reference value is determined based on a gain of an amplifier for amplifying said pixel signals corresponding to at least one frame of an image."**

Regarding claim 9, the prior art of record fails to teach or fairly suggest the combination of all limitations of claim 9 that includes **"said correction circuit further comprises an offset generation section which compares the pixel signals for each**

column with a reference value corresponding to brightness of at least one frame of an image, generates said offset for each column dynamically according to the result of the comparison, and updates the dynamically generated offset for each column as the offset for each column, wherein said reference value is determined based on a gain of an amplifier for amplifying said pixel signals corresponding to at least one frame of an image."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHAN T. TRAN whose telephone number is (571)272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nhan T. Tran/
Primary Examiner, Art Unit 2622